WHAT IS CLAIMED IS:

1. A method for texturing a semiconductor material, comprising the steps of:

(a) exposing at least part of a surface of the semiconductor material to an etching solution, such that said exposed part of said surface is contacted and wetted by said etching solution;

(b) negatively biasing the semiconductor material to a potential more negative than minus sixty volts relative to a standard reference electrode; and

(c) illuminating said exposed part of said surface contacted and wetted by said etching solution, during said negative biasing, for a period of time starting from initiation of said illuminating, such that value of cathodic current density of the semiconductor material is significantly higher at end of said illumination time period than at beginning of said illumination time period.

2. The method of claim 1, wherein the semiconductor material is selected from the group consisting of silicon (Si), germanium (Ge), and a combination thereof.

3. The method of claim 1, wherein the semiconductor material is an alloy selected from the group consisting of a silicon-germanium alloy, a silicon-carbon alloy, a germanium-carbon alloy, a silicon-nitrogen alloy, and a combination thereof.

4. The method of claim 1, wherein the semiconductor material is selected from the group consisting of a metal oxide, a metal phosphide, a metal sulfide, a metal arsenide, a metal selenide, a metal telluride, and a combination thereof.

5. The method of claim 1, wherein the semiconductor material includes a non-semiconductor material.

6. The method of claim 1, wherein doped conductive type of the semiconductor material is variable.

7. The method of claim 1, wherein the semiconductor material is a doped conductive type of silicon selected from the group consisting of a doped p-type silicon, a doped n-type silicon, and a combination thereof.

8. The method of claim 1, wherein grade of the semiconductor material is selected from the group consisting of a metallurgical grade and a semiconductor grade.

9. The method of claim 1, wherein geometrical configuration, shape, or form, of the semiconductor material is selected from the group consisting of amorphous, mono-crystalline, poly-crystalline, multi-crystalline, and a combination thereof.

10. The method of claim 9, wherein type of crystallinity or crystallographic orientation is variable for a said mono-crystalline, a said poly-crystalline, a said multi-crystalline, or a said combination thereof, type of said geometrical configuration, shape, or form, of the semiconductor material.

11. The method of claim 1, wherein the semiconductor material is silicon having a type of crystallinity or crystallographic orientation selected from the group consisting of <100>, <110>, and <111>.

12. The method of claim 1, wherein dimensions of the semiconductor material are selected from the group consisting of on order of sub-microns, on order of microns, on order of millimeters, on order of centimeters, on order of at least a meter, and a combination thereof.

13. The method of claim 1, wherein construction of the semiconductor material is selected from the group consisting of part of a single assembly, a composite of two or more parts of a single assembly, a single complete assembly, a composite of two or more single complete assemblies, and a combination thereof.

14. The method of claim 1, wherein construction of the semiconductor material is selected from the group consisting of part of a single wafer, a composite of two or more

parts of a single wafer, a single complete wafer, a composite of two or more single complete wafers, and a combination thereof.

15. The method of claim 1, wherein construction of the semiconductor material is selected from the group consisting of a thin film, a thick film, and a combination thereof.

16. The method of claim 1, wherein construction of the semiconductor material includes a substrate.

17. The method of claim 1, wherein the semiconductor material is in a non-masked form.

18. The method of claim 1, wherein the semiconductor material is in a masked form.

19. The method of claim 1, wherein the semiconductor material is in a polished form.

20. The method of claim 1, wherein the semiconductor material is in an as cut unpolished form.

21. The method of claim 1, wherein the semiconductor material is used for manufacturing a solar cell or a photovoltaic panel.

22. The method of claim 1, wherein type of said etching solution is selected from the group consisting of an acidic etching solution, a neutral etching solution, a basic or alkaline etching solution, and a molten etching solution.

23. The method of claim 22, wherein said acidic etching solution is an acidic aqueous solution selected from the group consisting of hydrofluoric acid (HF), nitric acid (HNO_3), phosphoric acid (H_3PO_4), and a combination thereof.

24. The method of claim 22, wherein said neutral etching solution is selected from the group consisting of a neutral aqueous solution including dissolved ions, and, an organic solution.

25. The method of claim 22, wherein said basic or alkaline etching solution is a basic or alkaline aqueous solution of an alkali hydroxide.

26. The method of claim 22, wherein said molten etching solution is a solution of a melted salt.

27. The method of claim 1, wherein concentration of solute in said etching solution is at least about 0.001 M.

28. The method of claim 1, wherein concentration of solute in said etching solution is in a range of between about 8 % (wt. solute / wt. solution) and about 50 % (wt. solute / wt. solution).

29. The method of claim 1, wherein temperature of said etching solution is in a range of between about freezing point of said etching solution and about boiling point of said etching solution.

30. The method of claim 1, wherein said etching solution is aqueous, and temperature of said aqueous etching solution is in a range of between about 20 °C and about 90 °C.

31. The method of claim 1, wherein said etching solution is aqueous, and temperature of said aqueous etching solution is in a range of between about 50 °C and about 90 °C.

32. The method of claim 1, wherein flow rate of said etching solution contacting and wetting said surface of the semiconductor material is in a range of between about 0 liter per minute and about 10 liters per minute.

33. The method of claim 1, wherein flow rate of said etching solution contacting and wetting said surface of the semiconductor material is in a range of between about 1 mL per minute and about 2.5 liters per minute.

34. The method of claim 1, wherein flow rate of said etching solution contacting and wetting said surface of the semiconductor material is in a range of between about 1 mL per minute and about 250 mL per minute.

35. The method of claim 1, wherein step (a) is performed for a period of time of at least about one minute prior to initiating step (b) of said negative biasing of the semiconductor material, such that said exposed part of said surface reaches a steady-state value of an open circuit potential (OCP) relative to said standard reference electrode.

36. The method of claim 1, wherein step (b), the semiconductor material is negatively biased to a said potential in a range of between more negative than minus sixty volts and about minus one hundred volts relative to said standard reference electrode.

37. The method of claim 1, wherein step (b), the semiconductor material is negatively biased to a said potential more negative than minus one hundred volts relative to said standard reference electrode.

38. The method of claim 1, wherein said negative biasing of step (b) is performed for a period of time of at least about one minute, prior to initiating said illuminating of step (c), such that the semiconductor material reaches a steady-state value of said applied negative potential relative to said standard reference electrode, and such that there is establishing a steady-state value of said cathodic current density of the semiconductor material.

39. The method of claim 1, wherein step (c), said illuminating is performed by a specifically controlled and directed light source which generates specifically controlled and directed-generated light in a form of non-ambient light.

40. The method of claim 39, wherein said specifically controlled and directed light source is selected from the group consisting of a halogen lamp, a tungsten-halogen lamp, and a dye laser.

41. The method of claim 39, wherein a specifically controlled and directed-processed light, in a form of processed said non-ambient light, is formed from intentional processing of said specifically controlled and directed-generated light, and is directed toward said exposed part of said surface of the semiconductor material.

42. The method of claim 41, wherein said specifically controlled and directed-generated light, together with said specifically controlled and directed-processed light, are specifically controlled and directed for producing said processed non-ambient light having an intensity of at least 0.01 watts per cm^2 at said negatively biased semiconductor material surface that is contacted and wetted by said etching solution.

43. The method of claim 41, wherein said specifically controlled and directed-generated light, together with said specifically controlled and directed-processed light, are specifically controlled and directed for producing said processed non-ambient light having an intensity in a range of between about 0.5 watts per cm^2 and about 5.0 watts per cm^2 at said negatively biased semiconductor material surface that is contacted and wetted by said etching solution.

44. The method of claim 41, wherein said specifically controlled and directed-processed light, incident upon said negatively biased semiconductor material surface that is contacted and wetted by etching solution, is light selected from the group consisting of polychromatic light, monochromatic light, poly- or multi-monochromatic light, and combinations thereof.

45. The method of claim 41, wherein said specifically controlled and directed-processed light, incident upon said negatively biased semiconductor material

surface that is contacted and wetted by etching solution, has a wavelength in a range of between about 100 nm and about 0.5 mm.

46. The method of claim 41, wherein said specifically controlled and directed-processed light, incident upon said negatively biased semiconductor material surface that is contacted and wetted by etching solution, has a wavelength in a range of between about 250 nm and about 1500 nm.

47. The method of claim 41, wherein said specifically controlled and directed-processed light, incident upon said negatively biased semiconductor material surface that is contacted and wetted by etching solution, has a wavelength in a range of between about 280 nm and about 500 nm.

48. The method of claim 1, wherein step (c), within about one second of initiating said illumination of said exposed part of said surface during said negative biasing, said value of said cathodic current density of the semiconductor material instantaneously increases to a value corresponding to that at said beginning of said illumination time period.

49. The method of claim 48, wherein during remainder of duration of said illumination time period, actual form and magnitude of said increase in said value of said cathodic current density of the semiconductor material from said value at said beginning of said illumination time period to said value at said end of said illumination time period, are functions of a combination of operating conditions and parameters being type of the semiconductor material; type, concentration, temperature, and flow rate, of said etching solution; magnitude and duration of said negative biasing; and intensity, wavelength, and duration, of said illumination incident upon said negatively biased semiconductor material surface.

50. The method of claim 1, wherein step (c), said period of time is about 60 seconds, starting from initiation of said illuminating.

51. The method of claim 1, wherein step (c), said period of time is about 600 seconds, starting from initiation of said illuminating.

52. The method of claim 1, wherein step (c), said period of time is about 5000 seconds, starting from initiation of said illuminating.

53. A method for texturing an as cut unpolished semiconductor material, comprising the steps of:

(a) exposing at least part of a surface of the as cut unpolished semiconductor material to an etching solution, such that said exposed part of said surface is contacted and wetted by said etching solution; and

(b) negatively biasing the as cut unpolished semiconductor material to a negative potential of at least minus one volt relative to a standard reference electrode for a period of time, during which the as cut unpolished semiconductor material is illuminated by light having an intensity of less than 0.01 watts per cm^2, such that value of cathodic current density of the as cut unpolished semiconductor material as a function of time during said time period initially increases to a maximum value, then decreases to a series of values each being significantly less than said maximum value.

54. The method of claim 53, wherein the as cut unpolished semiconductor material is selected from the group consisting of silicon (Si), germanium (Ge), and a combination thereof.

55. The method of claim 53, wherein the as cut unpolished semiconductor material is an alloy selected from the group consisting of a silicon-germanium alloy, a silicon-carbon alloy, a germanium-carbon alloy, a silicon-nitrogen alloy, and a combination thereof.

56. The method of claim 53, wherein the as cut unpolished semiconductor material is selected from the group consisting of a metal oxide, a metal phosphide, a metal sulfide, a metal arsenide, a metal selenide, a metal telluride, and a combination thereof.

57. The method of claim 53, wherein the as cut unpolished semiconductor material includes a non-semiconductor material.

58. The method of claim 53, wherein doped conductive type of the as cut unpolished semiconductor material is variable.

59. The method of claim 53, wherein the as cut unpolished semiconductor material is a doped conductive type of silicon selected from the group consisting of a doped p-type silicon, a doped n-type silicon, and a combination thereof.

60. The method of claim 53, wherein grade of the as cut unpolished semiconductor material is selected from the group consisting of a metallurgical grade and a semiconductor grade.

61. The method of claim 53, wherein geometrical configuration, shape, or form, of the as cut unpolished semiconductor material is selected from the group consisting of amorphous, mono-crystalline, poly-crystalline, multi-crystalline, and a combination thereof.

62. The method of claim 61, wherein type of crystallinity or crystallographic orientation is variable for a said mono-crystalline, a said poly-crystalline, a said multi-crystalline, or a said combination thereof, type of said geometrical configuration, shape, or form, of the as cut unpolished semiconductor material.

63. The method of claim 53, wherein the as cut unpolished semiconductor material is silicon having a type of crystallinity or crystallographic orientation selected from the group consisting of <100>, <110>, and <111>.

64. The method of claim 53, wherein dimensions of the as cut unpolished semiconductor material are selected from the group consisting of on order of sub-microns,

on order of microns, on order of millimeters, on order of centimeters, on order of at least a meter, and a combination thereof.

65. The method of claim 53, wherein construction of the as cut unpolished semiconductor material is selected from the group consisting of part of a single assembly, a composite of two or more parts of a single assembly, a single complete assembly, a composite of two or more single complete assemblies, and a combination thereof.

66. The method of claim 53, wherein construction of the as cut unpolished semiconductor material is selected from the group consisting of part of a single wafer, a composite of two or more parts of a single wafer, a single complete wafer, a composite of two or more single complete wafers, and a combination thereof.

67. The method of claim 53, wherein construction of the as cut unpolished semiconductor material is selected from the group consisting of a thin film, a thick film, and a combination thereof.

68. The method of claim 53, wherein construction of the as cut unpolished semiconductor material includes a substrate.

69. The method of claim 53, wherein the as cut unpolished semiconductor material is in a non-masked form.

70. The method of claim 53, wherein the as cut unpolished semiconductor material is in a masked form.

71. The method of claim 53, wherein the as cut unpolished semiconductor material is used for manufacturing a solar cell or a photovoltaic panel.

72. The method of claim 53, wherein type of said etching solution is selected from the group consisting of an acidic etching solution, a neutral etching solution, a basic or alkaline etching solution, and a molten etching solution.

73. The method of claim 72, wherein said acidic etching solution is an acidic aqueous solution selected from the group consisting of hydrofluoric acid (HF), nitric acid (HNO_3), phosphoric acid (H_3PO_4), and a combination thereof.

74. The method of claim 72, wherein said neutral etching solution is selected from the group consisting of a neutral aqueous solution including dissolved ions, and, an organic solution.

75. The method of claim 72, wherein said basic or alkaline etching solution is a basic or alkaline aqueous solution of an alkali hydroxide.

76. The method of claim 72, wherein said molten etching solution is a solution of a melted salt.

77. The method of claim 53, wherein concentration of solute in said etching solution is at least about 0.001 M.

78. The method of claim 53, wherein concentration of solute in said etching solution is in a range of between about 8 % (wt. solute / wt. solution) and about 50 % (wt. solute / wt. solution).

79. The method of claim 53, wherein temperature of said etching solution is in a range of between about freezing point of said etching solution and about boiling point of said etching solution.

80. The method of claim 53, wherein said etching solution is aqueous, and temperature of said aqueous etching solution is in a range of between about 20 °C and about 90 °C.

81. The method of claim 53, wherein said etching solution is aqueous, and temperature of said aqueous etching solution is in a range of between about 50 °C and about 90 °C.

82. The method of claim 53, wherein flow rate of said etching solution contacting and wetting said surface of the as cut unpolished semiconductor material is in a range of between about 0 liter per minute and about 10 liters per minute.

83. The method of claim 53, wherein flow rate of said etching solution contacting and wetting said surface of the as cut unpolished semiconductor material is in a range of between about 1 mL per minute and about 2.5 liters per minute.

84. The method of claim 53, wherein flow rate of said etching solution contacting and wetting said surface of the as cut unpolished semiconductor material is in a range of between about 1 mL per minute and about 250 mL per minute.

85. The method of claim 53, wherein step (a) is performed for a period of time of at least about one minute prior to initiating step (b) of said negative biasing of the as cut unpolished semiconductor material, such that said exposed part of said surface reaches a steady-state value of an open circuit potential (OCP) relative to said standard reference electrode.

86. The method of claim 53, wherein step (b), the as cut unpolished semiconductor material is negatively biased to a said negative potential in a range of between said at least minus one volt and about minus one hundred volts relative to said standard reference electrode.

87. The method of claim 53, wherein step (b), the as cut unpolished semiconductor material is negatively biased to a said negative potential in a range of between at least minus ten volts and about minus one hundred volts relative to said standard reference electrode.

88. The method of claim 53, wherein step (b), the as cut unpolished semiconductor material is negatively biased to a said negative potential in a range of between at least minus twenty volts and about minus fifty volts relative to said standard reference electrode.

89. The method of claim 53, wherein during said negative biasing time period, actual form and magnitude of said initial increase in said value of said cathodic current density of the as cut unpolished semiconductor material to said maximum value, then decrease in said value of said cathodic current density of the as cut unpolished semiconductor material to said series of said values each being significantly less than said maximum value, are functions of a combination of operating conditions and parameters of type of the semiconductor material; type, concentration, temperature, and flow rate, of said etching solution; and, magnitude and duration of said negative biasing.

90. The method of claim 53, wherein step (b), said period of time is in a range of between about 120 seconds and about 2100 seconds, starting from initiating of said negative biasing of the as cut unpolished semiconductor material.

91. The method of claim 53, wherein step (b) said illuminating is performed by a non-specifically controlled and directed light source which generates non-specifically controlled and directed-generated (unprocessed) light in a form of ambient light.

92. A method for texturing an as cut unpolished semiconductor material, consisting essentially of the steps of:

(a) exposing at least part of a surface of the as cut unpolished semiconductor material to an etching solution, such that said exposed part of said surface is contacted and wetted by said etching solution; and

(b) negatively biasing the as cut unpolished semiconductor material to a negative potential of at least minus one volt relative to a standard reference electrode for a period of time, such that value of cathodic current density of the as cut unpolished semiconductor material as a function of time during

said time period initially increases to a maximum value, then decreases to a series of values each being significantly less than said maximum value.

93. A textured semiconductor material, textured by the method comprising the steps of:

(a) providing a semiconductor material;

(b) exposing at least part of a surface of said semiconductor material to an etching solution, such that said exposed part of said surface is contacted and wetted by said etching solution;

(c) negatively biasing said semiconductor material to a potential more negative than minus sixty volts relative to a standard reference electrode; and

(d) illuminating said exposed part of said surface contacted and wetted by said etching solution, during said negative biasing, for a period of time starting from initiation of said illuminating, such that value of cathodic current density of said semiconductor material is significantly higher at end of said illumination time period than at beginning of said illumination time period.

94. The textured semiconductor material of claim 93, wherein morphology of at least part of said surface of the textured semiconductor material is characterized by presence of pyramids.

95. The textured semiconductor material of claim 93, wherein morphology of at least part of said surface of the textured semiconductor material is characterized by presence of inverted pyramids.

96. A textured as cut unpolished semiconductor material, textured by the method comprising the steps of:

(a) providing an as cut unpolished semiconductor material;

(b) exposing at least part of a surface of said as cut unpolished semiconductor material to an etching solution, such that said exposed part of said surface is contacted and wetted by said etching solution; and

(c) negatively biasing said as cut unpolished semiconductor material to a negative potential of at least minus one volt relative to a standard reference electrode for a period of time, during which said as cut unpolished semiconductor material is illuminated by light having an intensity of less than 0.01 watts per cm^2, such that value of cathodic current density of said as cut unpolished semiconductor material as a function of time during said time period initially increases to a maximum value, then decreases to a series of values each being significantly less than said maximum value.

97. The textured as cut unpolished semiconductor material of claim 96, wherein morphology of at least part of said surface of the textured as cut unpolished semiconductor material is characterized by presence of long prisms or coined triangles.

98. The textured as cut unpolished semiconductor material of claim 96, wherein morphology of at least part of said surface of the textured as cut unpolished semiconductor material is a function of crystal orientation of the as cut unpolished semiconductor material.

99. A textured as cut unpolished semiconductor material, textured by the method consisting essentially of the steps of:

(a) providing an as cut unpolished semiconductor material;

(b) exposing at least part of a surface of said as cut unpolished semiconductor material to an etching solution, such that said exposed part of said surface is contacted and wetted by said etching solution; and

(c) negatively biasing said as cut unpolished semiconductor material to a negative potential of at least minus one volt relative to a standard reference electrode for a period of time, such that value of cathodic current density of said as cut unpolished semiconductor material as a function of time during said time period initially increases to a maximum value, then decreases to a series of values each being significantly less than said maximum value.

100. The textured as cut unpolished semiconductor material of claim 99, wherein morphology of at least part of said surface of the textured as cut unpolished semiconductor material is characterized by presence of long prisms or coined triangles.

101. The textured as cut unpolished semiconductor material of claim 99 wherein morphology of at least part of said surface of the textured as cut unpolished semiconductor material is a function of crystal orientation of the as cut unpolished semiconductor material.